

# UMI0028\_I

## ISPI30I USB OTG Transceiver Eval Kit User's Guide

Semiconductors

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### User's Guide Rev. 1.0

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## 1. Introduction

The ISP1301 is a Universal Serial Bus (USB) On-The-Go (OTG) transceiver device that is fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0*. It integrates a USB full-speed and low-speed transceiver, and other analog components to fully support OTG functionality.

The ISP1301 is ideal for use in portable electronics devices, such as mobile phones, personal digital assistants (PDAs), digital still cameras, and digital audio players. The ISP1301 acts as a physical layer to interface with any USB OTG Controller.

The ISP1301 evaluation board is designed to evaluate the functions of the ISP1301 chip. The main components on the board are: the ISP1301 (in HVQFN24 package), I<sup>2</sup>C master, USB mini-AB connector, analog audio interface, and USB OTG controller interface. The operation mode of the ISP1301 can be configured through the I<sup>2</sup>C interface. The OTG status and control registers in the ISP1301 can also be accessed through the I<sup>2</sup>C interface.

To verify the functions of the ISP1301 by using the DOS test program that is provided with the evaluation kit, connect the ISP1301 evaluation board to the parallel port of a PC. To fully verify the functions of the ISP1301, a USB OTG controller is used to connect to the ISP1301 board through the defined interface connector.

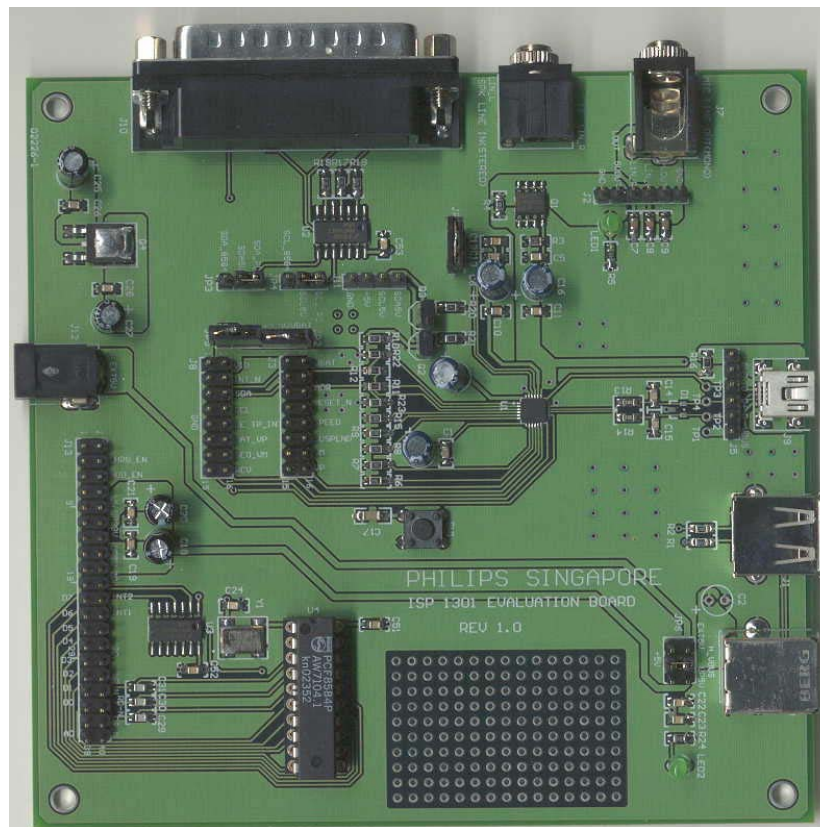


Figure 1-1: ISP1301 evaluation board PCB layout

## 2. System requirements

An x86 PC with DB-25 parallel port is required. The test program runs on DOS (or the command line in Microsoft® Windows® 98). In the BIOS setting, select port address 378H for the onboard parallel port. The test program is compiled using Turbo® C++ 3.0.

### 3. Configurations and settings

#### 3.1. Power requirements

By default, the ISPI301 board is powered by a +5.0 V power supply through the DC jack (J12, inner +). The +5.0 V power can also be supplied from the USB Type-B connector (J4). However, when J4 is connected to a USB port on the PC, leave the USB mini-AB connector (J9) unconnected. If an external microprocessor is used to control the I<sup>2</sup>C controller chip PCF8584 (U4), the +5.0 V power can also be supplied from pin 16 and pin 18 of the microprocessor connector (J13).

When the +5.0 V power is correctly applied to the board, LED2 (green) will turn ON.

Table 3-1: +5.0 V power selection

Jumper	Descriptions
JP6	<b>Short 1 (UP5V) and 2 (+5V):</b> +5.0 V from the microprocessor interface (pin 16 or 18 of J13) <b>Short 3 (H_VBUS) and 4 (+5V):</b> +5.0 V from the V <sub>BUS</sub> line of the USB connector (pin 1 of J4) <b>Short 5 (EXT5V) and 6 (+5V):</b> +5.0 V from the DC jack (J12, inner +) [default]

The power supply (V<sub>BAT</sub> pin) for the ISPI301 can be provided either from the onboard +3.3 V source or from the OTG Controller interface (pin 2 of J3).

Similarly, the power supply for the V<sub>IO</sub> (called V<sub>DD\_LGC</sub> in the ISPI301 datasheet) pin of the ISPI301 can be provided either from the onboard +3.3 V source or from the OTG Controller interface (pin 2 of J8).

Table 3-2: V<sub>BAT</sub> and V<sub>IO</sub> selection

Jumper	Descriptions
JP2	<b>Short:</b> V <sub>BAT</sub> from the onboard +3.3 V source [default] <b>Open:</b> V <sub>BAT</sub> from the pin 2 of J3
JP5	<b>Short:</b> V <sub>IO</sub> from the onboard +3.3 V source [default] <b>Open:</b> V <sub>IO</sub> from the pin 2 of J8

#### 3.2. I<sup>2</sup>C master selection

The I<sup>2</sup>C master controller can be supplied from any one of three sources:

- PC parallel port (software I<sup>2</sup>C master)
- Philips I<sup>2</sup>C controller chip PCF8584 (hardware I<sup>2</sup>C master)
- External I<sup>2</sup>C master that is connected to the I<sup>2</sup>C header J11.

Table 3-3: I<sup>2</sup>C master selection

Jumper	Descriptions
JP3	<b>Short 1 (SDA_8584) and 2 (SDA5V):</b> SDA from PCF8584 <b>Short 2 (SDA5V) and 3 (SDA_PC):</b> SDA from PC parallel port [default] <b>Open:</b> SDA from I <sup>2</sup> C connector (pin 4 of J11)
JP4	<b>Short 1 (SCL_8584) and 2 (SCL5V):</b> SCL from PCF8584 <b>Short 2 (SCL5V) and 3 (SCL_PC):</b> SCL from PC parallel port [default] <b>Open:</b> SCA from I <sup>2</sup> C connector (pin 3 of J11)

**Note:** SCL and SDA come from the same I<sup>2</sup>C master.

### 3.3. USB interface

There are three USB connectors on the ISPI301 evaluation board.

- If an OTG Controller is connected to the ISPI301, the USB port functions as an OTG dual-role device and only the mini-AB connector (J5) will be used.
- If a Host Controller is connected to the ISPI301, the USB port functions as a host and only the Type-A connector (J1) will be used.
- If a Device Controller is connected to the ISPI301, the USB port functions as a device and only the Type-B connector (J4) will be used.

You can use all the three ports at the same time. If you have a system that consists of a USB host port and a separate device port, then the host port can be connected to J4 and the device port can be connected to J1 using the standard USB cable. In such a case, the ISPI301 provides only OTG functions to the system; the transceiver function of the ISPI301 is not used.

### 3.4. Audio interface

The ISPI301 evaluation board has an interface to support an analog audio carkit application. Connect:

- The audio carkit to the mini-AB connector (J9) on the board;
- The audio input line signal to the SPK LINE IN socket (J6) on the board;
- The audio output line signal to the MIC LINE OUT socket (J7) on the board.

### 3.5. Reset

For a hardware reset to the ISPI301, press the manual reset switch (SW1). The reset pulse (active LOW) can also come from the OTG Controller interface (pin 8 of J3).

## 4. Location of major components

Figure 4-1 shows the location of major components on the evaluation board.

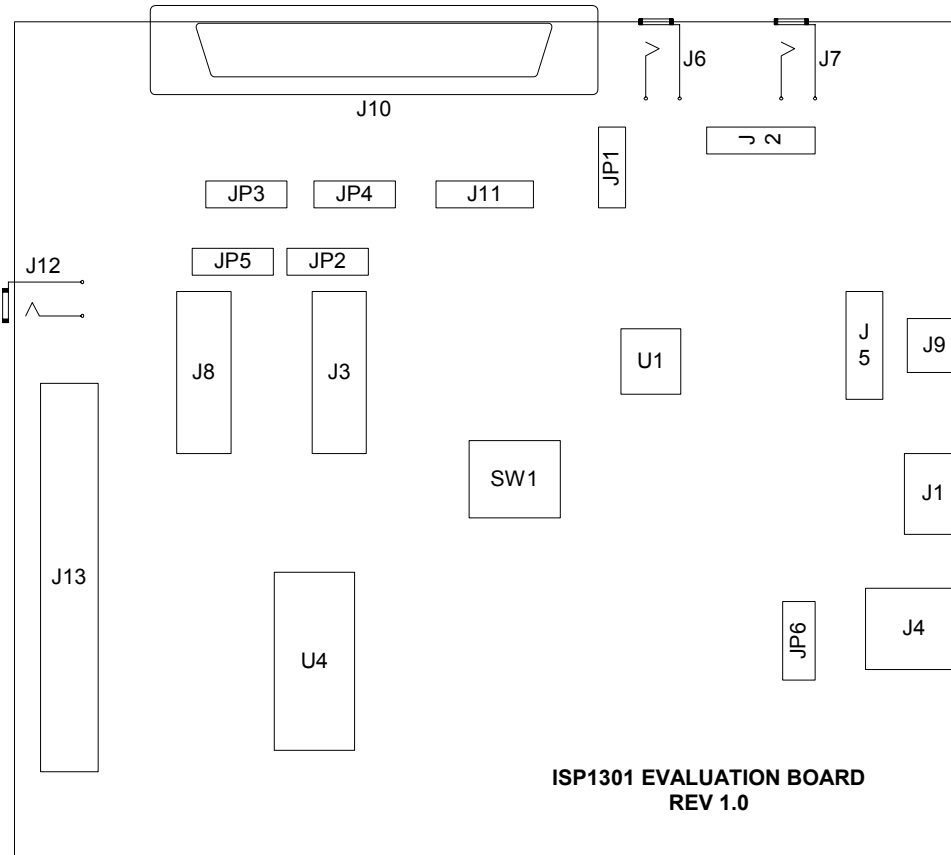


Figure 4-1: Location of major components

## 5. Test program I301.EXE

### 5.1. Introduction

A DOS test program "I301.exe" is provided to help you verify the functions of the ISP1301 chip. The program uses the PC parallel port to access the ISP1301 registers through the I<sup>2</sup>C interface. The program simulates software I<sup>2</sup>C master at the hardware abstraction layer (HAL).

The test program can do the following:

- Set the I<sup>2</sup>C slave address for the ISP1301 based on the hardware setting of the ADR pin
- Reset all registers to their default values
- Display the current value of all registers on your PC screen
- Write any value to a writable register
- Set the mode of operation of the ISP1301 (such as, USB function and suspend mode, transparent I<sup>2</sup>C mode, transparent general-purpose buffer mode, and global power-down mode)
- Enable or disable the charge pump of the ISP1301.



## 5.2. Running the test program

If your PC boots to pure DOS, run the test program on the command line. If your PC boots to Microsoft Windows 98, open an MS-DOS window and run the test program. It is recommended that you boot the PC to pure DOS.

To run the test program, type **I301**<sup>1</sup> and press the **Enter** key at the command prompt.

**Note:** In the BIOS setting of the PC, the I/O address for the onboard parallel port is 378H.

## 5.3. Using menus

After the program has been launched, the main menu will appear on the screen. See Figure 5-1.

```

MS-DOS Prompt - 1301
=====
ISP1301 OTG Xcvr Test Program Ver0.9
(c)2002 Philips Semiconductors - APIC
=====
***** Main Menu *****
1: Choose I2C slave address for ISP1301
2: Reset all registers
3: List all registers
4: Read/Write register
5: Select Mode of Operation
6: Enable/Disable charge-pump

Esc: exit
select:

```

Figure 5-1: Test program main menu

In the main menu screen, selecting any item 1–6 will perform the desired action. If you wish to exit the program, press the **Esc** key.

The following sections describe the menu items.

### 5.3.1. Choose I2C slave address for ISP1301

The program will prompt you to enter your choice based on the hardware setting of the ADR pin.

- If ADR is HIGH, select 1. The slave address for the ISP1301 will become 0x5A.
- If ADR is LOW, select 0. The slave address for the ISP1301 will become 0x58.

Make sure that choices are done correctly; otherwise, other operations may fail.

If you set the ISP1301 to the transparent I<sup>2</sup>C mode and choose a slave address value other than the value set here, you must set it back to the original slave address when you revert to the direct I<sup>2</sup>C mode.

### 5.3.2. Reset all registers

On selecting this option, the program will set all the registers—excluding the read-only registers—to their default values and display these values on your PC screen.

<sup>1</sup> In this document, items that you type or click are indicated in **bold**.

### 5.3.3. List all registers

On selecting this option, the program will display all the 22 registers on the screen. See Figure 5-2.

```

MS-DOS Prompt - 1301
Auto
ISP1301 register values:
=====
Address Description          Value  Default value
=====
0x00-01 Vendor ID           0x04CC default = 0x04CC
0x02-03 Product ID         0x1301 default = 0x1301
0x14-15 Chip Version       0x0100 default = 0x0100
0x04/05 Mode Control 1     0x00   default = 0x00
0x12/13 Mode Control 2     0x04   default = 0x04
0x06/07 OTG Control 1      0x0C   default = 0x0C
0x08   Interrupt source    0xA0   default = 0xA0
0x0A/0B Interrupt Latch    0x00   default = 0x00
0x0C/0D Interrupt Enable 0 0x00   default = 0x00
0x0E/0F Interrupt Enable 1 0x00   default = 0x00

Press any key to return to previous menu:_

```

Figure 5-2: List all registers screen display

### 5.3.4. Read/Write register

The program will display the current value of all registers and prompt you to write to a specific register.

On selecting item 4 from the main menu, the program will display the screen given in Figure 5-3. The program will prompt you to type the address of the register whose value you want to change. On entering the address of the register and pressing Enter, the program will prompt you to enter the new value that you want to assign. If you want to return to the main menu, type **FF** at the command prompt.

```

MS-DOS Prompt - 1301
ISP1301 register values:
=====
Address Description          Value   Default value
=====
0x00-01 Vendor ID           0x04CC default = 0x04CC
0x02-03 Product ID         0x1301 default = 0x1301
0x14-15 Chip Version       0x0100 default = 0x0100
0x04/05 Mode Control 1     0x00   default = 0x00
0x12/13 Mode Control 2     0x04   default = 0x04
0x06/07 OTG Control 1      0x0C   default = 0x0C
0x08   Interrupt Source    0xA0   default = 0xA0
0x0A/0B Interrupt Latch    0xFF   default = 0x00
0x0C/0D Interrupt Enable 0 0x00   default = 0x00
0x0E/0F Interrupt Enable 1 0x00   default = 0x00

Enter register address to write(enter FF to exit): 0x0B
Enter register value to write: 0xFF_

```

Figure 5-3: Read/Write register screen display

### 5.3.5. Select Mode of Operation

You can select the mode of operation of the ISP1301 by selecting item 5 from the main menu. A submenu will appear on the screen. See Figure 5-4. The possible choices include the USB functional mode (four data encoding and decoding methods), transparent I<sup>2</sup>C mode, transparent buffer mode, USB suspend mode, and global power-down mode.

**Note:** If the ISP1301 Engineering Sample I (ESI) (that is, the chip whose version register reads 0x0100, or the chip package is marked #####AX) is mounted on the evaluation board, software cannot wake up the chip, if set to the global power-down mode. Only a hardware reset can wake up the chip.

```

MS-DOS Prompt - 1301
***** Mode Menu *****
1: USB functional Mode
2: Transparent I2C Mode
3: Transparent Buffer Mode
4: USB Suspend Mode Enable/Disable
5: Global Power Down Mode Enable/Disable
6: List Current Mode

Esc: return to previous menu
Select:

```

Figure 5-4: Select Mode of Operation screen display

### 5.3.6. Enable/Disable charge-pump

If the charge pump in the ISP1301 is disabled, selecting menu item 6 will enable the charge pump. If the charge pump is enabled, selecting menu item 6 will disable it.

## 6. Hardware description

### 6.1. Block diagram

Figure 6-1 shows the block diagram of the ISPI301 evaluation board.

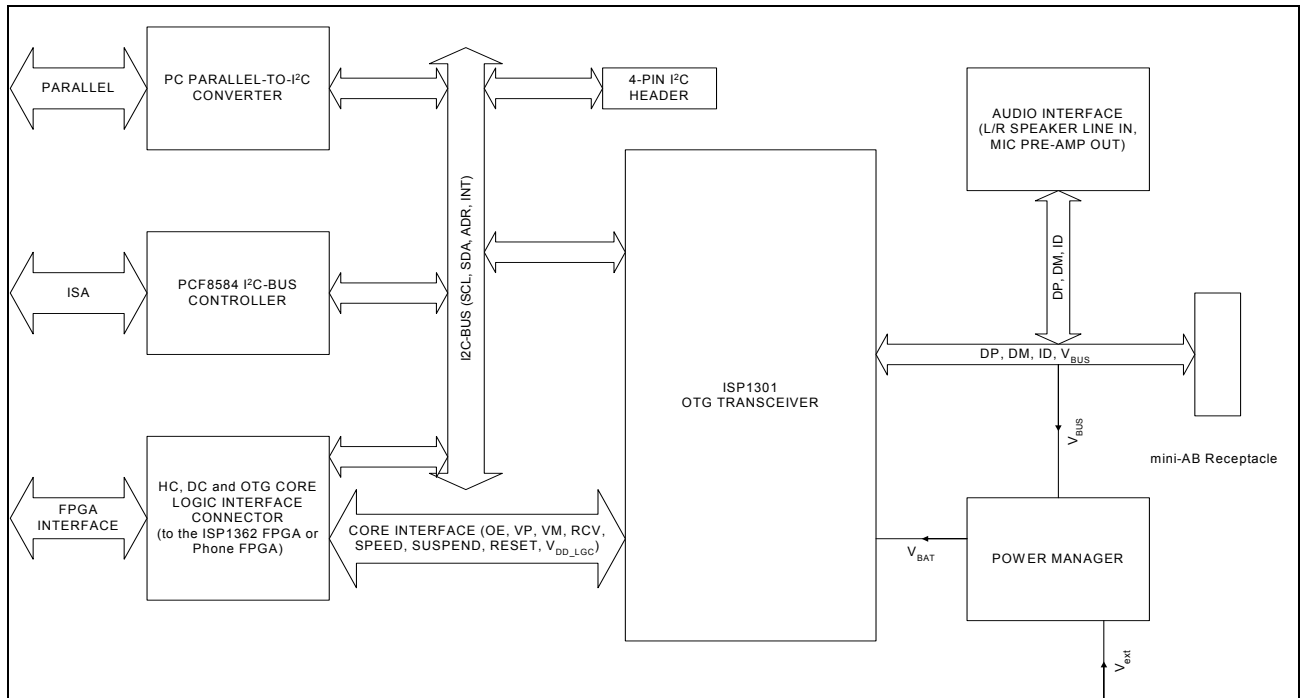


Figure 6-1: Block diagram of the ISPI301 evaluation board

### 6.2. Functional description

A brief description of each function module is given in the following sections.

#### 6.2.1. PCF8584 I<sup>2</sup>C-bus controller

This block provides functions of the I<sup>2</sup>C-bus to the 8-bit parallel-bus converter. It can connect to the Philips ISPI362 or ISPI161x ISA interface board, or any other generic 8-bit microprocessor interface through a 40-wire IDE cable. The PC or other microprocessor can service the interrupt from the ISPI301 and access the registers of the ISPI301 through this interface.

#### 6.2.2. PC parallel to I<sup>2</sup>C converter

This interface provides an alternative method to access the ISPI301 I<sup>2</sup>C interface through the PC. The PC needs to emulate software I<sup>2</sup>C master to access the ISPI301 I<sup>2</sup>C slave.

#### 6.2.3. HC, DC and OTG core logic interface connector

This interface provides connection to a Host Controller (HC), Device Controller (DC) or On-The-Go (OTG) core logic. This interface is used during OTG system-level evaluation or during compliance testing.

### 6.2.4. Power manager

This block includes the 5.0 V-to-3.3 V regulator and power source selection.

### 6.2.5. Audio interface

This block provides stereo audio line IN interface and microphone (with pre-amp) OUT interface. Its main purpose is to demonstrate the carkit application (play audio or voice with carkit).

## 7. Connector pin information

### 7.1. DB-25 PC parallel port connector (J10) pin assignment

J10 is used to connect to the PC parallel port through the DB-25 printer cable. Table 7-1 shows its pin assignment.

Table 7-1: DB-25 PC parallel port connector (J10) pin assignment

Pin no	Printer port signal	ISPI301 evaluation board signal
9	D7	SDAOUT#
11	S7#	SDAIN#
15	S3	SCLIN
17	C3#	SCLOUT#
10,13,18–25	—	GND
1–8,12,14,16,	—	No connection

### 7.2. 8-bit microprocessor interface 20 x 2 header (J13) pin assignment

J13 is used to connect to a generic 8-bit parallel bus microprocessor controller. The bus uses the Intel® mode. Required signals include D0–D7, A0, WR\_N, RD\_N, CS\_N, INT1 and INT2. Table 7-2 shows the pin assignment for J13.

**Note:** We use a 20 x 2 header to make it compatible with the Philips ISPI362 and ISPI161x ISA interface boards.

Table 7-2: 8-bit microprocessor-interface 20 x 2 header (J13) pin assignment<sup>[1]</sup>

Pin no	Pin name	Pin no	Pin name	Pin no	Pin name	Pin no	Pin name
1	GND	11	n. c.	21	D7	31	D2
2	n. c.	12	+3.3 V	22	INT2	32	n. c.
3	n. c.	13	n. c.	23	D6	33	D1
4	CHRG_EN	14	n. c.	24	INT1	34	WR_N
5	n. c.	15	n. c.	25	D5	35	D0
6	n. c.	16	+5.0 V	26	n. c.	36	RD_N
7	n. c.	17	n. c.	27	D4	37	n. c.
8	n. c.	18	+5.0 V	28	n. c.	38	CS_N
9	n. c.	19	GND	29	D3	39	A0
10	+3.3 V	20	n. c.	30	n. c.	40	n. c.

[1] n. c.—Denotes no connection.

**Note:** An external OTG Controller system can use the CHRG\_EN signal to enable or disable +5.0 V from the V<sub>BUS</sub> line of the mini-AB connector to pin 2 of J2. This is useful when an analog audio carkit is attached and the carkit can charge the external battery.

### 7.3. USB OTG Controller interface 8 x 2 header (J8 and J3) pin assignment

Header connectors J8 and J3 are used to connect the ISPI301 to the OTG Controller core. J8 includes the USB Serial Interface Engine (SIE) signals—DAT\_VP, SE0\_VM, RCV and OE\_TP\_INT\_N—and I<sup>2</sup>C signals—SDA, SCL and INT\_N. J3 also includes other signals that may be used by selected OTG Controller.

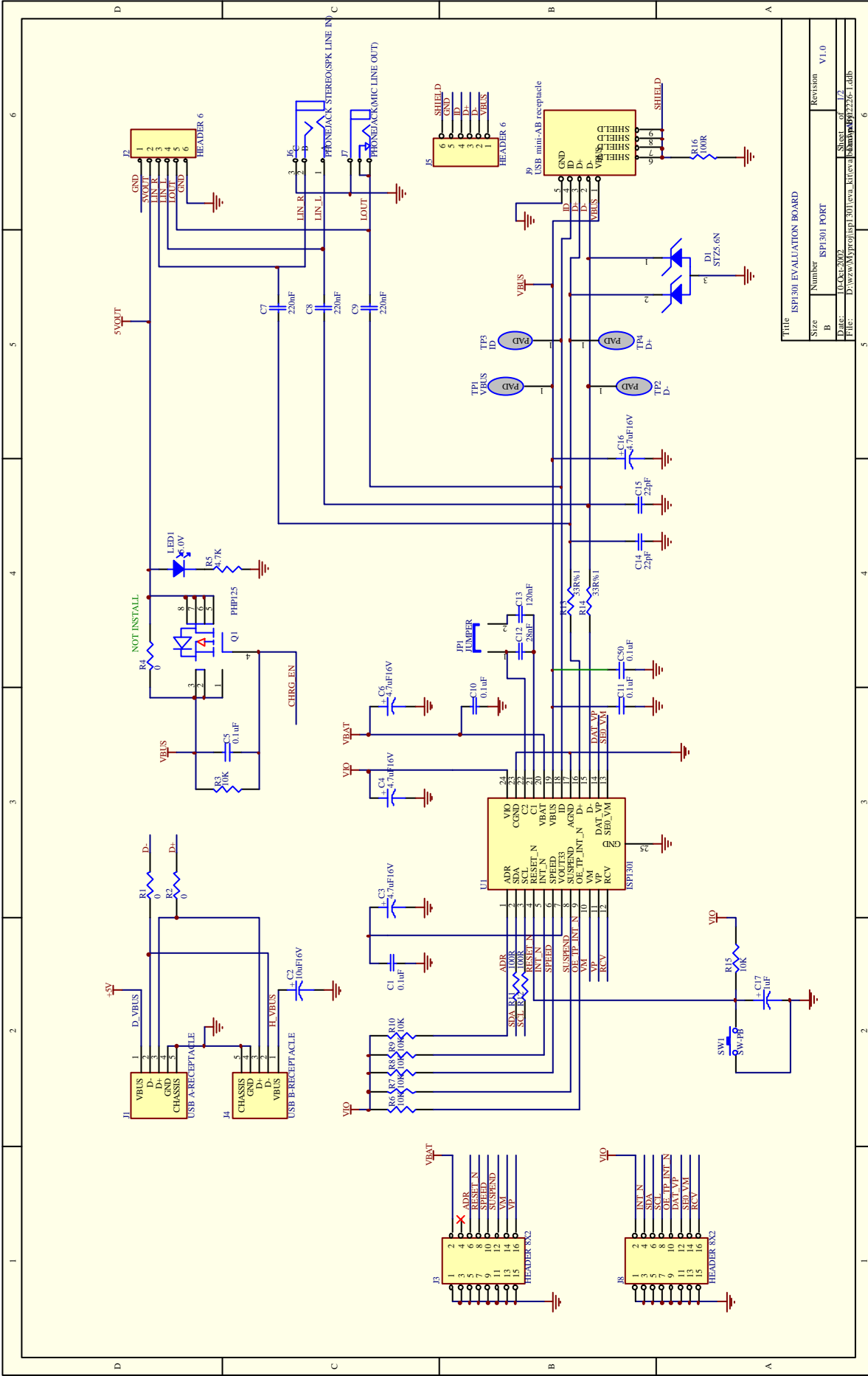
Table 7-3: OTG Controller interface J8 pin assignment

Pin no	Pin name	Pin no	Pin name
1	GND	9	GND
2	V <sub>IO</sub>	10	OE_TP_INT_N
3	GND	11	GND
4	INT_N	12	DAT_VP
5	GND	13	GND
6	SDA	14	SE0_VM
7	GND	15	GND
8	SCL	16	RCV

Table 7-4: OTG Controller interface J3 pin assignment

Pin no	Pin name	Pin no	Pin name
1	GND	9	GND
2	V <sub>BAT</sub>	10	SPEED
3	GND	11	GND
4	n. c.	12	SUSPEND
5	GND	13	GND
6	ADR	14	VM
7	GND	15	GND
8	RESET_N	16	VP

## 8. Schematics of the evaluation board



Title		ISP300 EVALUATION BOARD	
Size	Number	ISP300 PORT	Revision
B			V1.0
FILE:	DATE:	DESIGNED BY:	REVISED BY:
ISP300.PCB	2007-12-19	WANG, KUN	WANG, KUN
FILE:	DATE:	DESIGNED BY:	REVISED BY:
ISP300.PCB	2007-12-19	WANG, KUN	WANG, KUN

1 2 3 4 5 6

1 2 3 4 5 6

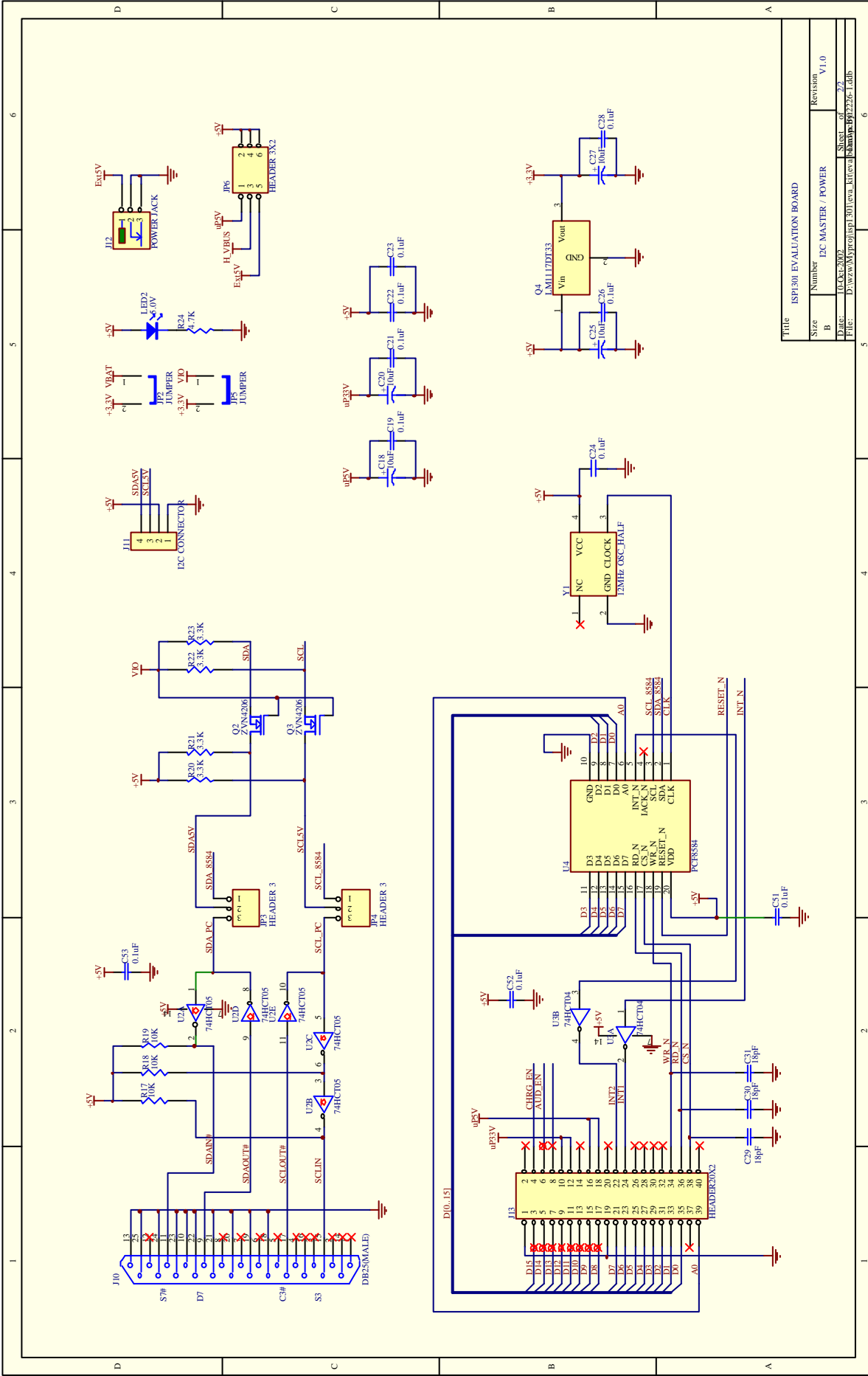
1 2 3 4 5 6

1 2 3 4 5 6

1 2 3 4 5 6

1 2 3 4 5 6

1 2 3 4 5 6



Title			
Size	Number	I2C MASTER / POWER	Revision
B			V1.0
Date:	UCC:2007	Sheet	2
File:	D:\work\byproduct\isp130\evm_kit\pcb\main\isp130_2222_1.dtb	Sheet	2

Title			
Size	Number	I2C MASTER / POWER	Revision
B			V1.0
Date:	UCC:2007	Sheet	2
File:	D:\work\byproduct\isp130\evm_kit\pcb\main\isp130_2222_1.dtb	Sheet	2

Title			
Size	Number	I2C MASTER / POWER	Revision
B			V1.0
Date:	UCC:2007	Sheet	2
File:	D:\work\byproduct\isp130\evm_kit\pcb\main\isp130_2222_1.dtb	Sheet	2

Title			
Size	Number	I2C MASTER / POWER	Revision
B			V1.0
Date:	UCC:2007	Sheet	2
File:	D:\work\byproduct\isp130\evm_kit\pcb\main\isp130_2222_1.dtb	Sheet	2

Title			
Size	Number	I2C MASTER / POWER	Revision
B			V1.0
Date:	UCC:2007	Sheet	2
File:	D:\work\byproduct\isp130\evm_kit\pcb\main\isp130_2222_1.dtb	Sheet	2

Title			
Size	Number	I2C MASTER / POWER	Revision
B			V1.0
Date:	UCC:2007	Sheet	2
File:	D:\work\byproduct\isp130\evm_kit\pcb\main\isp130_2222_1.dtb	Sheet	2

Title			
Size	Number	I2C MASTER / POWER	Revision
B			V1.0
Date:	UCC:2007	Sheet	2
File:	D:\work\byproduct\isp130\evm_kit\pcb\main\isp130_2222_1.dtb	Sheet	2



## 9. Bill of Materials

Table 9-1: BOM of the ISPI301 evaluation board

Part Type	Quantity	Designator	Footprint
18pF +80%/-20%	3	C29, C30, C31	0805
22pF ±10%	2	C14, C15	0805
28nF ±10%	1	C12	0805
120nF ±10%	1	C13	0805
220nF ±10%	3	C7, C8, C9	0805
0.1uF+80%/-20%	11	C1, C5, C10, C11, C19, C21, C22, C23, C24, C26, C28	0805
1uF+80%/-20%	1	C17	1206
4.7uF16V	4	C3, C4, C6, C16	RB.1/.2
10uF16V	5	C2, C18, C20, C25, C27	RB.1/.2
0R	3	R1, R2, R4	0805
33R ±%1	2	R13, R14	0805
100R	3	R11, R12, R16	0805
3.3K	4	R20, R21, R22, R23	0805
4.7K	2	R5, R24	0805
10K	10	R3, R6, R7, R8, R9, R10, R15, R17, R18, R19	0805
12MHz OSC_HALF	1	Y1	XTAL-CTX
ISPI301	1	U1	HVQFN24
74HCT05	1	U2	SOP14
74HCT04	1	U3	SOP14
PCF8584 I2C CONTROLLER	1	U4	DIP20
PHPI25 P-MOSFET POWER MOS	1	Q1	SO8
ZVN4206 N-MOSFET	2	Q2, Q3	TO92
LMI117DT33 3.3V REGULATOR	1	Q4	TO252
STZ5.6N ESD DIODE	1	D1	SOT346
LED	2	LED1, LED2	Thru'hole
DB25 (MALE)	1	J10	Thru'hole
HEADER 3	2	JP3, JP4	Thru'hole
HEADER 4	1	J11	Thru'hole
HEADER 3X2	1	JP6	Thru'hole
HEADER 6	2	J2, J5	Thru'hole
HEADER 8X2	2	J3, J8	Thru'hole
HEADER20X2	1	J13	Thru'hole
JUMPER	3	JP1, JP2, JP5	Thru'hole
PHONEJACK (MIC LINE OUT)	1	J7	PHONEJACK
PHONEJACK STEREO (SPK LINE IN)	1	J6	PHONEJACK STEREO
POWER JACK	1	J12	DC JACK
SW-PB	1	SW1	SW-TACT
USB A-RECEPTACLE	1	J1	USB A
USB B-RECEPTACLE	1	J4	USB B
USB mini-AB RECEPTACLE	1	J9	USB mini-AB

## 10. References

- *ISP1301 USB On-The-Go Transceiver* datasheet
- *Universal Serial Bus Specification Rev. 2.0*
- *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0*
- *ISP1301 Errata*